WEST Search History

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	DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L29	L28 same control$4	8	L29
L28	L24 same hysteresis	14	L28
L27	L25 same hysteresis	0	L27
L26	L25 same switch$4	20	L26
L25	l23 same L24	53	L25
L24	((plurality or multiple) adj2 reference adj2 voltages)	1215	L24
L23	L22 same comparator	6785	L23
L22	(voltage adj2 generator)	45056	L22
L21	(request adj2 message) same (response adj2 message) same ((shar$4) adj2 (buffer or queue or fifo))	1	L21
L20	(request adj2 message) same (response adj2 message) same ((one or single) adj2 (buffer or queue or fifo))	5	L20
L19	L18.ab.	28	L19
L18	(request adj2 (buffer or queue or fifo)) same (response adj2 (buffer or fifo or queue))	217	L18
L17	l14.ab.	1	L17
L16	L14 same pool	1	L16
L15	L14 and l9	0	L15
L14	L13 same shar$4	32	L14
L13	(request adj2 (buffer or queue or memory or fifo)) same (response adj2 (buffer or fifo or queue or memory))	572	L13
L12	l8 same pool	1	L12
L11	l8.ab.	24	L11
L10	l9 and l8	0	L10
L9	((710/56)!.CCLS.)	252	L9
L8	L7 same shar$4	104	L8
L7	(request near2 (buffer or queue or memory or fifo)) same (response near2 (buffer or fifo or queue or memory))	1711	L7
L6	(non-i/o near3 data)	6	L6
L5	(distinguish$4 near3 non-i/o near3 data)	0	L5
L4	L2.ab.	13	L4
L3	L2 same (i/o or (input/output))	1	L3
L2	L1 same (message near2 type near2 (id or ident$7))	82	L2
L1	((transmit$4 or send$4 or transfer$4) near2 data)	371564	L1

L26: Entry 5 of 20 File: USPT May 8, 2001

DOCUMENT-IDENTIFIER: US 6229472 B1
TITLE: A/D converter

Abstract Text (1):
An A/D converter for converging an input analogue signal to a digital signal includes a reference voltage generator, a comparator and an encoder. The comparator comparing a plurality of reference voltages with the input analogue signal includes a first switch to which the analogue signal is input, an array of second switches connected between the reference voltages and a charge capacitor, and a comparator having an input connected to the charge capacitor and an output connected to the input of the comparator, and an encoder for encoding an output signal of the comparator.

Brief Summary Text (16):
The present invention provides, in a first aspect thereof, an A/D converter for converting an input analogue signal to a digital signal comprising: a reference voltage generator for generating a plurality of reference voltages; a comparator for comparing the plurality of the reference voltages with the input analogue signal, the comparator including a first switch having a first terminal connected to an analogue input terminal, an array of second switches each having a first terminal connected to the corresponding reference voltage and a second terminal connected in common to a second terminal of the first switch, a charge capacitor having a first terminal connected to second terminals of the first switch and of the array of the second switches, and an amplifier having an input connected to a second terminal of the charge capacitor and an output connected to the input of said comparator by a third switch; and an encoder for encoding an output signal of the comparator.

CLAIMS:

2. The A/D converter as defined in claim 1, wherein said converter includes a plurality of said comparators, and a plurality of said reference voltages generated in said reference voltage generator are input to the respective comparators by way of the array of said second switches.

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L26: Entry 1 of 20 File: USPT Dec 10, 2002

DOCUMENT-IDENTIFIER: US 6493125 B1
TITLE: Apparatus for stabilizing light source frequency

Detailed Description Text (39):
The delay time detector 7 is formed by the mixer MIX1 and the lowpass filter LPF1. To the mixer MX1, output of the switch SW2 is applied. Output of the mixer MX1 is coupled to the comparator R1. A plurality of reference voltage Vr1 to Vrn are provided in the reference voltage generator 9. Each reference voltage is assigned to each channel, respectively. Further, the reference voltage generator 9 has a switch SW4 for coupling one of the reference voltages to the mixer MIX1. The switch SW4 is operated according to the selecting signal applied from the switch controller 5.

L26: Entry 4 of 20 File: USPT Aug 28, 2001

DOCUMENT-IDENTIFIER: US 6281828 B1
TITLE: Analog/digital converter apparatus

Detailed Description Text (15):
An input signal is supplied to one terminal of each of the plural comparator sections 4 from the input terminal 1, and a plurality of reference voltages are generated from the reference voltage generator 3 and each applied to the other terminal of the comparator section 4. In the first mode, the MOS transistors M1 and M4 of the signal switching section 6 of each comparator section 4 are turned on, and the MOS transistors M2 and M3 thereof are turned off, and the input signal and reference voltage are input to the differential amplifier 7. The output of the differential amplifier 7 is then held in the sample hold circuit of the subtracter 8.

L26: Entry 8 of 20 File: USPT Sep 22, 1998

DOCUMENT-IDENTIFIER: US 5812079 A
TITLE: Subranging type A/D converter apparatus equipped with feedback line for transmitting control signal for A/D conversion

Abstract Text (1):
In a subranging type A/D converter apparatus, the A/D converter apparatus executes A/D conversion by separating the A/D conversion into an A/D conversion of high-order bits and an A/D conversion of low-order bits in two steps, while feeding back a first control signal for executing the A/D conversion of the low-order bits according to results of the A/D conversion of the high-order bits. A digital logic circuit section executes decision of the A/D conversion to a control terminal of a switch group of a reference voltage generator circuit for generating a plurality of reference voltages via a feedback line provided in a plurality of voltage comparators provided with a plurality of differential amplifiers. Each of the differential amplifiers includes a plurality of transistors each for executing differential amplification. The plurality of differential amplifier transistors are arranged so as to be symmetrical with respect to the feedback line provided in each of the differential amplifiers.

Brief Summary Text (30):
In order to achieve the above-mentioned objective, according to one aspect of the present invention, there is provided a subranging type analog-to-digital converter apparatus for executing analog-to-digital conversion by separating the analog-to-digital conversion into an analog-to-digital conversion of high-order bits and an analog-to-digital conversion of low-order bits in two steps, while feeding back a first control signal for executing the analog-to-digital conversion of the low-order bits according to results of the analog-to-digital conversion of the high-order bits, from a digital logic circuit section for executing decision of the analog-to-digital conversion to a control terminal of a switch group of a reference voltage generator circuit for generating a plurality of reference voltages via a feedback line provided in a plurality of voltage comparators provided with a plurality of differential amplifiers,

Detailed Description Text (72):
As described above in detail, according to the preferred embodiments of the present invention, there can be provided a subranging type A/D converter apparatus which executes A/D conversion by separating the A/D conversion into an A/D conversion of high-order bits and an A/D conversion of low-order bits in two steps while feeding back the first control signal for executing the A/D conversion of the low-order bits according to the results of A/D conversion of the high-order bits, from a digital logic circuit section for executing the decision of the A/D conversion to the control terminal of the switch group of the reference voltage generator circuit for generating a plurality of reference voltages via the feedback line provided in a plurality of voltage comparators provided with a plurality of differential amplifiers, wherein each of the differential amplifiers is provided with a plurality of transistors for executing differential amplification, and the plurality of transistors are arranged so as to be symmetrical with respect to the feedback line provided in each of the differential amplifiers. With the above arrangement, the influence of a voltage fluctuation on the feedback line for transmitting the control signal for executing the switching control of the switch group on the input and output lines and the transistor elements are reduced, thereby suppressing the possible deterioration of the operational accuracy of each of the differential amplifiers to improve the A/D conversion performance.

CLAIMS:

1. A subranging type analog-to-digital converter apparatus for executing analog-to-digital conversion by separating the analog-to-digital conversion into an analog-to-digital conversion of high-order bits and an analog-to-digital conversion of low-order bits in two steps, while feeding back a first control signal for executing the analog-to-digital conversion of the low-order bits according to results of the analog-to-digital conversion of the high-order bits, comprising:

a digital logic circuit section for executing decision of the analog-to-digital conversion and sending the decision, via a feedback line provided in conjunction with a plurality of voltage comparators having a plurality of differential amplifiers, to a control terminal of a switch group of a reference voltage generator circuit for generating a plurality of reference voltages,

wherein each of said differential amplifiers includes a plurality of transistors each for executing differential amplification, and

wherein said plurality of transistors are arranged so as to be symmetrical with respect to said feedback line provided in conjunction with each of said differential amplifiers.

L29: Entry 1 of 8 File: USPT Apr 18, 2000

DOCUMENT-IDENTIFIER: US 6051994 A
TITLE: Variable voltage driver

Brief Summary Text (6):
IBM patented a "Precision Hysteresis Circuit" by B. L. Stakely and R. Wenda, with U.S. Pat. No. 5,122,680, for a CMOS circuit arrangement with precise balanced switch points. The circuit arrangement included a voltage-follower which forces a reference voltage across an on-chip reference resistor. The current which is generated is mirrored and is made to flow through a plurality of on-chip resistors. The mirrored current flowing through the plurality of resistors generates a plurality of proportional reference voltages. Two of the proportional reference voltages are used to set the switching threshold to one input of a comparator whose output is fed back to control a switch which selects one of the two voltages. Another one of the proportional reference voltages is coupled to another input of the comparator. The circuit arrangement forms a hysteresis circuit if positive and negative thresholds are chosen. Generating hysteresis on an integrated circuit chip generated a a precise voltage across an on-chip resistance, and current mirroring provided a current (IREF) flowing in the on-chip resistance (R0) to flow in a plurality of ratioed independent resistive means. Then a fixed voltage is generated across a selected one of the ratioed independent resistive means and compared with a selected one of a plurality of switched voltages generated across selected ones of the ratioed independent resistance. However, these ideas did not address a growing and current problem which needs to be addressed as complex machines are developed which migrate some components among successive machines as when new machines use newer technologies (migrating from one CMOS process which could be and has been called a Level 5, to a more dense, higher level, such as a level 6 process or technology) with lower signal swings. As an example in a situation addressed by the preferred embodiment of my invention in newer S/390 machines the off multichip module (MCM) memory paths are 2.5V signals, while it needs to couple to a cache of one technology which operates at 2.5V for one machine while a related machine developed with a different technology may need a 1.8V signal. The development of a separate 1.8V memory interface for the related machine is costly. There is a need to improve the circuits in multiple technology chip crossings to ease migratable machines allowing older technology circuits to be used in a new generation of machines without having to remake the circuits for a new technology and having to incur the consequent development costs, which could be in the million dollar range

L29: Entry 2 of 8 File: USPT Feb 1, 2000

DOCUMENT-IDENTIFIER: US 6020767 A
TITLE: CMOS chip to chip settable interface receiver cell

Brief Summary Text (5):
Later IBM patented a "Precision Hysteresis Circuit" by B. L. Stakely and R. Wenda, with U.S. Pat. No. 5,122,680, for a CMOS circuit arrangement with precise balanced switch points. The circuit arrangement included a voltage-follower which forces a reference voltage across an on-chip reference resistor. The current which is generated is mirrored and is made to flow through a plurality of on-chip resistors. The mirrored current flowing through the plurality of resistors generates a plurality of proportional reference voltages. Two of the proportional reference voltages are used to set the switching threshold to one input of a comparator whose output is fed back to control a switch which selects one of the two voltages. Another one of the proportional reference voltages is coupled to another input of the comparator. The circuit arrangement forms a hysteresis circuit if positive and negative thresholds are chosen. Generating hysteresis on an integrated circuit chip generated a precise voltage across an on-chip resistance, and current mirroring provided a current (IREF) flowing in the on-chip resistance (R0) to flow in a plurality of ratioed independent resistive means. Then a fixed voltage is generated across a selected one of the ratioed independent resistive means and compared with a selected one of a plurality of switched voltages generated across selected ones of the ratioed independent resistance.

L29: Entry 7 of 8 File: USPT Jun 16, 1992

DOCUMENT-IDENTIFIER: US 5122680 A
TITLE: Precision hysteresis circuit

Abstract Text (1):
Described is a CMOS circuit arrangement with precise balanced, differential switch points. The circuit arrangement includes a voltage-follower which forces a reference voltage across an on-chip reference resistor. The current which is generated is mirrored and is made to flow through a plurality of on-chip resistors. The mirrored current flowing through the plurality of resistors generate a plurality of proportional reference voltages. Two of the proportional reference voltages are used to set the switching threshold to one input of a comparator whose output is fed back to control a switch which selects one of the two voltages. Another one of the proportional reference voltages is coupled to another input of the comparator. The circuit arrangement forms a hysteresis circuit if positive and negative thresholds are chosen.